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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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06/02/1998

STEWART FINDLATER

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EXAMINER

HOM, SHICK C

ART UNIT

PAPER NUMBER

2666

DATE MAILED: 04/02/2004

36

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/089,312

**Applicant(s)**

FINDLATER ET AL.

**Examiner**

Shick C Hom

**Art Unit**

2666

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 20 January 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-17, 19 and 20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-17, 19-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

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**DETAILED ACTION**

***Response to Arguments***

1. Applicant's arguments filed 1/20/04 have been fully considered but they are not persuasive.

In page 5 line 28 to page 6 line 18 applicant argued that Muller et al. fails to teach that the receive data valid signal being received onto the same pin as the receive error signal and the transmit enable signal being transmitted on the same control pin as the transmit error signal are not persuasive; although Muller et al. uses three separate pins to multiplex the transmit signals TxD0, TxD1, TxD2 with the TxD3, TxEN, TxER signals; and three separate pins to multiplex the receive signals RxD0, RxD1, RxD2 with the RxD3, RxDV, RxER signals, col. 6 lines 33-41 which recite that these signals can be multiplexed in a variety of ways clearly anticipate the receive data valid signal, RxDV, being multiplex and received onto the same pin as the receive error signal, RxER, and the transmit enable signal, TxEN, being multiplex and transmitted on the same control pin as the transmit error signal, TxER.

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***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Muller et al. (6,044,087).

Regarding claims 15 and 16:

Muller et al. disclose the interface between a first media access control layer and a second media access control layer (col. 4 line 57 to col. 5 line 4), consisting essentially of: a common clock (col. 5 lines 5-43); a time-division multiplexed receive data line (col. 5 lines 5-24); a time-division multiplexed receive control line for transmitting different functional types of receive control signals including a receive data valid signal and a receive error signal (see Figs. 4a-b,

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and col. 6 lines 8-47); a time-division multiplexed transmit data line (col. 7 lines 18-37); a time-division multiplexed transmit control line for transmitting different functional types of transmit control signals including a transmit enable signal and a transmit error signal (see Figs. 3a-b, col. 5 line 53 to col. 6 line 7, and col. 6 lines 33-47).

Regarding claim 17:

Muller et al. disclose wherein said time-division multiplexed receive control line contains receive control signals further comprising a carrier sense signal (col. 5 lines 25-43).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

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claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-10 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (6,044,087) in view of official notice as indicated below.

Regarding claim 1:

Muller et al. disclose the method of communicating between a media access control layer (MAC) and a physical layer (PHY) (col. 4 line 57 to col. 5 line 4), comprising: sending a first 100 MHz time-division multiplexed signal on a receive data line (although Muller et al. did not recite a 100 MHz signal, col. 1 lines 46-61 which recite signals transmitted in compliance with the IEEE 802.3 standard and official notice is taken that it is well known the IEEE 802.3 protocol suite, commonly known as Ethernet, has a 100 Mbps throughput); sending a plurality of

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time-division multiplexed receive control signals on a receive control line (col. 5 lines 5-24); sending a second 100 MHz time-division multiplexed signal on a transmit data line (see col. 7 lines 18-37 which recite signals transmitted in compliance with the IEEE 802.3 standard and official notice being taken that it is well known the IEEE 802.3 protocol suite, commonly known as Ethernet, has a 100 Mbps throughput); sending a plurality of time-division multiplexed transmit control signals on a transmit control line (col. 5 lines 5-24), wherein the receive control signals include a receive data valid signal and a receive error signal (see Figs. 4a-b and col. 6 lines 8-47) and the transmit control signals include a transmit enable signal and a transmit error signal (see Figs. 3a-b, col. 5 line 53 to col. 6 line 7, and col. 6 lines 33-47).

Regarding claim 2:

Muller et al. disclose wherein the time-division multiplexed receive control signals includes 4 bit segments (although Muller et al. did not recite 4 bit segments, see col. 5 line 53 to col. 6 line 32 which recite transmitting and receiving control signals having nibbles of data and official notice is taken that it is well known nibbles are 4 bit segments) and wherein each 4 bit segment includes a synchronization bit (col. 5 lines 25-43).

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Regarding claim 3:

Muller et al. disclose wherein the receive data line includes 4 bit segments (col. 5 line 53 to col. 6 line 32 which recite transmitting and receiving control signals having nibbles of data and official notice is taken that it is well known nibbles are 4 bit segments) and wherein the beginning of a 4 bit segment of the receive data line is determined by the synchronization bit (col. 5 lines 25-43).

Regarding claim 4:

Muller et al. disclose wherein the time-division multiplexed receive control signals includes 4 bit segments of the receive data line and wherein each 4 bit segment includes a receive data valid bit (col. 5 line 53 to col. 6 line 32, Figs. 4a-b, and col. 6 lines 8-47).

Regarding claim 5:

Muller et al. disclose wherein the time-division multiplexed receive control signals includes 4 bit segments and wherein each 4 bit segment includes a receive error bit (col. 5 line 53 to col. 6 line 32, Figs. 4a-b, and col. 6 lines 8-47).

Regarding claim 6:

Muller et al. disclose wherein the time-division multiplexed receive control signals includes 4 bit segments and

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wherein each 4 bit segment includes a carrier sense bit (col. 5 line 53 to col. 6 line 32, Figs. 4a-b, and col. 5 lines 25-43).

Regarding claim 7:

Muller et al. disclose wherein the time-division multiplexed transmit control signals includes 4 bit segments of the transmit data line and wherein each 4 bit segment includes a synchronization bit (col. 5 line 53 to col. 6 line 32 and col. 5 lines 25-43).

Regarding claim 8:

Muller et al. disclose wherein the transmit data line includes 4 bit segments and wherein the beginning of a 4 bit segment of the transmit data line is determined by the synchronization bit (col. 5 line 53 to col. 6 line 32 and col. 5 lines 25-43).

Regarding claim 9:

Muller et al. disclose wherein the time-division multiplexed transmit control signals includes 4 bit segments and wherein each 4 bit segment includes a transmit enable bit (col. 5 line 53 to col. 6 line 32, Figs. 3a-b, col. 5 line 53 to col. 6 line 7, and col. 6 lines 33-47).

Regarding claim 10:

Muller et al. disclose wherein the time-division multiplexed transmit control signals includes 4 bit segments and

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wherein each 4 bit segment includes a transmit error bit (col. 5 line 53 to col. 6 line 32, Figs. 3a-b, col. 5 line 53 to col. 6 line 7, and col. 6 lines 33-47).

Regarding claims 19 and 20:

Muller et al. disclose wherein the receive control signals further include a synchronization (SYNC) signal and a carrier sense signal (col. 5 lines 25-43).

7. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (6,044,087) in view of Lese et al. (4,761,800).

For claims 11-12 Muller et al. disclose the method described in paragraph 7 of this office action. Muller et al. disclose all the subject matter of the claimed invention with the exception of indicating the speed of the PHY using the receive data line includes including an interface speed bit in a data segment when a receive control segment indicates no carrier sense, no receive data valid and no receive error as in claims 11-12.

Lese et al. from the same or similar fields of endeavor teach that it is known to provide the step of indicating the speed of the PHY using the receive data line includes including

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an interface speed bit in a data segment when a receive control segment indicates no carrier sense, no receive data valid and no receive error (col. 2 lines 16-44). Thus, it would have been obvious to the person having ordinary skill in the art at the time the invention was made to provide the step of indicating the speed of the PHY using the receive data line includes including an interface speed bit in a data segment when a receive control segment indicates no carrier sense, no receive data valid and no receive error as taught by Lese et al. in the method of Muller et al. The motivation for providing the step of indicating the speed of the PHY using the receive data line includes including an interface speed bit in a data segment when a receive control segment indicates no carrier sense, no receive data valid and no receive error as taught by Lese et al. in the method of Muller et al. being that it provides an improved asynchronous interface for coupling data between devices to achieve proper data speed matching in the method of Muller et al.

8. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (6,044,087) in view of Chow et al. (6,169,742).

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For claims 13-14 Muller et al. disclose the method described in paragraph 7 of this office action. Muller et al. disclose all the subject matter of the claimed invention with the exception of buffering data transmitted from the PHY to the MAC using an elasticity buffer that is at least 27 bits long as in claim 13 and buffering data transmitted from the PHY to the MAC using an elasticity buffer that long enough to buffer an entire frame of data from a data source having a clock with a frequency tolerance of 0.1% as in claim 14.

Chow et al. from the same or similar fields of endeavor teach that it is known to provide the step of buffering data transmitted from the PHY to the MAC using an elasticity buffer that is at least 27 bits long (col. 6 lines 9-27) and that is long enough to buffer an entire frame of data from a data source having a clock with a frequency tolerance of 0.1% (see Fig. 3a and col. 6 lines 9-27). Thus, it would have been obvious to the person having ordinary skill in the art at the time the invention was made to provide the step of buffering data transmitted from the PHY to the MAC using an elasticity buffer that is at least 27 bits long and that is long enough to buffer an entire frame of data from a data source having a clock with a frequency tolerance of 0.1% as taught by Chow et al. in the method of Muller et al. The motivation for providing the step

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of buffering data transmitted from the PHY to the MAC using an elasticity buffer that is at least 27 bits long and that is long enough to buffer an entire frame of data from a data source having a clock with a frequency tolerance of 0.1% as taught by Chow et al. in the method of Muller et al. being that it provides a more robust method of sending and receiving data packets and said more robust packet switching being desirable to achieve more efficient system operation in Muller et al.

### **Conclusion**

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action

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10. Any response to this final action should be mailed to:

Box AF

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306, (for formal communications;  
please mark "EXPEDITED PROCEDURE")

Or:

(for informal or draft communications, please  
label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal  
Park II, 2121 Crystal Drive, Arlington. VA., Sixth  
Floor (Receptionist).

Any inquiry concerning this communication or earlier  
communications from the examiner should be directed to Shick Hom  
whose telephone number is (703) 305-4742. The examiner's  
regular work schedule is Monday to Friday from 8:00 am to 5:30  
pm EST and out of office on alternate Friday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao, can be reached at (703) 308-5463.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.



TERENCE BOWMAN

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March 24, 2004